Remarks

This is responsive to the Office Action mailed February 7, 2008. Claims 1-18 and 21-25 are pending. Claims 6-14 are allowed and claims 1-5 and 15-25 stand rejected. Claims 1, 16 and 21 have been amended.

Applicant thanks the Examiner for the teleconference of April 23, 2008, with attorney David G. Woodral. This amendment is intended to be reflective of the issues discussed during the call and to serve as a formal filing of the draft claim amendments.

Rejection Under 35 U.S.C. §102

Claims 1-3, 5, 16, 18, and 21-24 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,457,787 to Asano et al. (Asano).

Claim 1 has been amended to recite in part: (a) retrieving a first portion of the recorded data via the bus in response to a first read command; (b) updating some of the registers via the bus in response to a zone transition event during the first read command; and (c) retrieving a second portion of the recorded data via the bus in response to the first read command.

In the Official Action, the Examiner stated regarding Asano's argued anticipation of claim 1 that "step (a) may be the completion of a first read command, step (b) sets the parameters for a subsequent read command, and step (c) is the start of the subsequent read command." Owing to the amendments to claim 1, it is now clear that all of the retrieved data is in response to a single first read command. Secondly, the step of updating some of the registers occurs in response to a zone transition event. Therefore, Asano can no longer be interpreted to anticipate claim 1. Therefore allowance of claim 1

is respectfully requested. Claims 2-3 depend from and further limit independent claim 1 and should also be allowable.

Independent claim 16 was rejected under the same reasoning as claim 1. Claim 16 has been amended to recite in part: (a) providing data from a storage medium via a bus, the bus operatively connected to at least one register, the storage medium, and a controller chip; (b) updating the at least one register or parameter via the bus in response to a zone transition event; and (c) continuing providing data from the storage medium via the bus responsive to the updating.

It is now clear that claim 16 updates at least one register or parameter in response to a zone transition event, which is neither taught nor suggested by Asano. Responsive to the update, claim 16 requires continuing providing data (rather than executing another command) from the storage medium, which is also neither taught nor suggested by Asano. Therefore claim 16 should be allowable. Claims 17-18 depend from and further limit independent claim 16 and should therefore be allowable as well.

Claim 21 was once again rejected under the same reasoning as claim 1. Claim 21 has been amended and now recites: A method for reducing processing burden on a processing device, comprising steps of transmitting first data in response to a read comment from a storage medium via a bus coupled to the processing device, updating at least one register or parameter via the bus in response to a zone transition event, and transmitting second data in response to the read command from the storage medium via the bus in response to the updating step.

The amendments clarify that a single read command is being executed, in contrast to Asano, which requires at least two read commands to anticipate claim 21.

Furthermore, Asano does not teach that updating of the registers is in response to a zone transition event as is now required by claim 21. Therefore claim 21 should be allowable. Claims 22-25 depend from and further limit independent claim 21 and should also be allowable.

Rejection of Claims Under 35 U.S.C. §103

Claim 15 stands rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,457,787 to Asano et al. (Asano) in view of U.S. Patent No. 5,438,665 to Taniai et al. (Taniai).

The Applicant respectfully traverses this rejection because the Examiner has failed to establish a *prima facie* case of obviousness because the references do not combine to teach the claimed limitations. Independent claim 15 recites in part, "a bus operatively coupled between the interface and the chips, the bus controllable by the DMA controller to read from the memory and to update several of the registers in response to a zone transition event."

Neither Asano nor Taniai teach or suggest that a zone transition event results in a bus updating several of the registers. For this reason, at least, a *prima facie* case of obviousness has not been made, and claim 15 should be allowable.

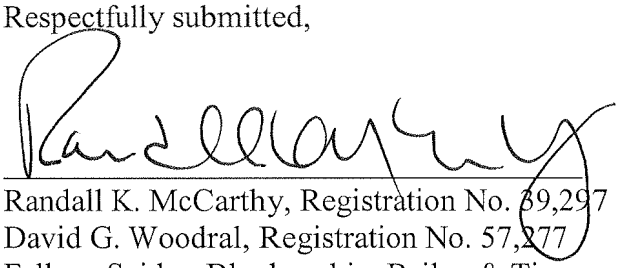
Allowable Subject Matter

The Applicant gratefully acknowledges the allowance of claims 6-14.

Conclusion

This is believed to be a complete response to the Office Action of February 7, 2008. Reconsideration and allowance of all pending claims is respectfully requested. Should the Examiner have any questions regarding this response, or can see any reason that the remaining claims should not be allowed, he is invited to telephone the below signed attorney.

Respectfully submitted,

By: 

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